REMARKS/ARGUMENTS

The Examiner is thanked for the courteous telephone interview granted Applicants' representative on June 19, 2007. During the interview, Applicants' representative proposed amending claim 1 to incorporate subject matter currently recited in claim 3 in an effort to place the case in condition for allowance. The Examiner indicated that such an amendment would appear to distinguish over the cited art if claim 1 was further amended to avoid use of alternative language currently recited in claim 3. The Examiner also indicated, however, that further searching and/or consideration was required and advised that the amended claim should be presented in an RCE application.

Claims 1, 2, 4-7, 11, 12, 14-19 and 21-25 are pending in the present application. Claims 1, 4, 11, 14, 18 and 21 were amended, and claims 3, 8-10, 13 and 20 were canceled. Claim 25 was added. Applicants have carefully considered the cited art and the Examiner's comments, and believe the claims patentably distinguish over the cited art and are allowable in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

I. Objections

The Examiner has required that all copending applications in the "Cross Reference to Related Applications" be properly identified. Applicants believe, however, that the appropriate information was previously provided in a Preliminary Amendment filed July 27, 2004.

II. 35 U.S.C. § 103, Obviousness: Claims 1-2, 5, 7-12, 15, 17-19, 22, and 24

The Examiner has finally rejected claims 1-2, 5, 7-12, 15, 17-19, 22, and 24 under 35 U.S.C. § 103(a) as being unpatentable over *Matsubara* et al., U.S. Patent No. 6,381,679 B1 (hereinafter "*Matsubara*") in view of Anonymously Disclosed, Method for the Dynamic Prediction of Nonsequential Memory Accesses, September 25, 2002 (hereinafter "*Anon*").

By the present Amendment, independent claim 1 has been amended to incorporate the subject matter previously recited in dependent claim 3, and independent claims 11 and 18 have been amended in a similar manner. Claims 8-10 have been canceled. This rejection, accordingly, is now moot.

III. 35 U.S.C. § 103, Obviousness: Claims 3, 13 and 20

The Examiner has finally rejected claims 3, 13, and 20 under 35 U.S.C. § 103(a) as being unpatentable over *Matsubara* in view of *Anon* as applied to claims 1 and 11 above, and in further view of

IBM Technical Disclosure, Cache Miss Director – A Means of Prefetching Cache Missed Lines (hereinafter IBMTD). This rejection is respectfully traversed.

The Examiner states:

> **As per claims 3 and 20,** the combination of Matsubara/Anon discloses all the limitations of claims 3 and 20 except determining whether outstanding cache misses are present;
>
> and prefetching the data if a number of outstanding cache misses are less than a threshold.
>
> IBMTD discloses determining whether outstanding cache misses are present (Discourse Text, lines 13-14); *It should be noted that the "demand miss" is analogous to the "cache miss."*
>
> and prefetching the data if a number of outstanding cache misses are less than a threshold (Discourse Text, lines 14-17). *It should be noted that this limitation contains language that suggests or makes optional but does not require steps to be performed or does not limit the claim to a particular structure and therefore does not limit the scope of a claim. The term 'if' denotes an optionally recited limitation and optionally recited limitations are not guaranteed to take place. Thus, simply "prefetching the data" is disclosed because the optionally recited parts of this limitation are not required to be taught by the Office. See MPEP §2106, Section II(C)). It should also be noted that "anticipatory cache misses" are analogous to "prefetching data."*
>
> The combination of Matsubara/Anon and IBMTD are analogous art because they are from the same field of endeavor, that being prefetching memory systems.
>
> At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement IBMTD's Cache Miss Directory (CMD) within Matsubara/Anon's information processing system.
>
> The motivation for doing so would have been to get the lines into the cache before a demand miss occurs for them, thus, reducing processing delays (IBMTD, Discourse Text, lines 2-3 and 19-20).
>
> Therefore, it would have been obvious to combine Matsubara, Anon, and IBMTD for the benefit of obtaining the invention as specified in claims 3 and 20.

Final Office Action dated March 22, 2007, pages 9 and 10.

Amended claim 1 is as follows:

> 1. A method in a data processing system for providing hardware assistance to prefetch data during execution of code by a processor in the data processing system, the method comprising:
>
> responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction; and
>
> responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor, wherein the selectively prefetching step includes:
>
> determining whether outstanding cache misses are present; and
>
> prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold.

For reasons discussed in detail previously, Applicants respectfully submit that neither *Matsubara*, nor *Anon*, nor their combination teaches or suggests "responsive to loading an instruction in the code into a

cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction" or "responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor" as recited in claim 1.

Matsubara describes that one or a plurality of "indication bits" can be provided in either an operation code or in an operand address of a software prefetch instruction for indicating the content of a prefetch operation. As described in Col. 5, lines 11-24 of *Matsubara*, such indication bits can indicate such things as at least one of a hierarchical level of a cache to which the operation data is to be prefetched and a quantity of the operation data to be prefetched. In *Matsubara*, a value of the indication bits indicates the operation to be performed.

Matsubara does not, however, disclose or suggest that a determination is made "whether a prefetch indicator is associated with the instruction" or that such a determination is made by a processor "responsive to loading an instruction in the code into a cache" as required by claim 1.

Matsubara also does not disclose or suggest "responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor" as recited in claim 1. Although *Matsubara* may disclose prefetching data in accordance with a value of a software prefetch instruction, this is not the same as selectively prefetching a pointer to a data structure identified by a prefetch indicator "responsive to the prefetch indicator being associated with the instruction".

Anon does not supply these deficiencies in *Matsubara*. Therefore, *Matsubara* in view of *Anon* still fails to teach or suggest "responsive to loading an instruction in the code into a cache, determining, by a processor unit, whether a prefetch indicator is associated with the instruction" or "responsive to the prefetch indicator being associated with the instruction, selectively prefetching a pointer to a data structure identified by the prefetch indicator into the cache in the processor" as recited in claim 1.

In addition, and as indicated above, the independent claims have been amended to incorporate the subject matter previously recited in dependent claims 3, 13 and 20, and the claims have been further amended to avoid use of the word "if" and to positively recite "prefetching the data in response to a determination that a number of outstanding cache misses is less than a threshold." In view of this amendment, the subject matter of the clause must be fully be considered by the Examiner, and as is believed to have been acknowledged by the Examiner during the above-referenced interview, IBMTD does not disclose or suggest this limitation. Independent claims 1, 11 and 18, accordingly, patentably distinguish over the references in their present form for this reason, as well.

For at least all the above reasons, independent claims 1, 11 and 18 patentably distinguish over the cited art and are allowable in their present form. Claims 2, 5, 7, 12, 14, 15, 17, 19, 22 and 24 depend from

and further restrict one of independent claims 1, 11 and 18 and also patentably distinguish over the cited art, at least by virtue of their dependency.

New claim 25 has been added to more fully protect Applicants' invention, and also patentably distinguishes over the cited art in its present form.

IV. 35 U.S.C. § 103, Obviousness: Claims 4, 6, 16, 21 and 23

The Examiner has rejected claims 4, 6, 16, 21, and 23 under 35 U.S.C. § 103(a) as being unpatentable over *Matsubara* in view of *Anon* as applied to claims 1 and 11 above, and in further view of *Malik*, U.S. Patent No. 6,687,794 B2. This rejection is respectfully traversed.

Claims 4, 6, 16, 21, and 23 depend from and further restrict one of claims 1, 11 and 18. *Malik* does not supply the deficiencies in *Matsubara*, *Anon* or IBMTD as described above. Claims 4, 6, 16, 21 and 23, accordingly, patentably distinguish over the references and are allowable in their present form, at least by virtue of their dependency.

With respect to claims 4, 14 and 21, in particular, the claims have been amended to avoid use of optional language. *Malik* does not disclose the subject matter of claims 4, 14 and 21 and these claims patentably distinguish over the cited art and are allowable in their own right as well as by virtue of their dependency.

V. Conclusion

For at least all the above reasons, Applicants believe that the subject application is patentable over the cited references and is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

/Gerald H. Glanzman/

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